

FIG. 1
PRIOR ART

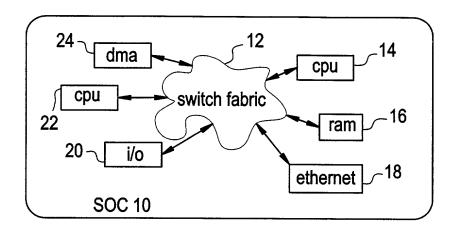


FIG. 2

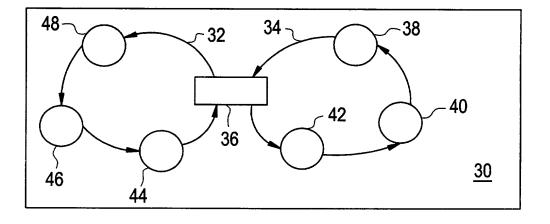




FIG. 3

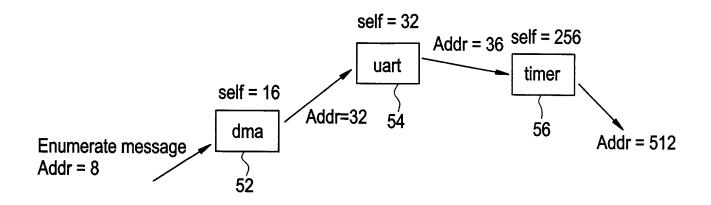


FIG. 4

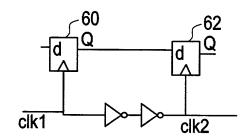


FIG. 5

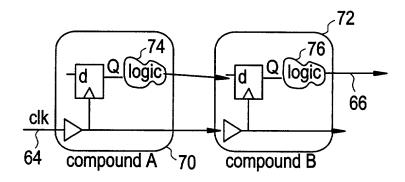




FIG. 6

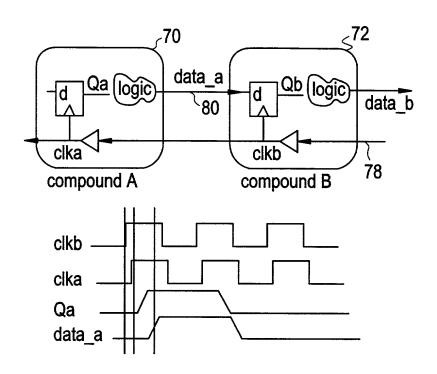
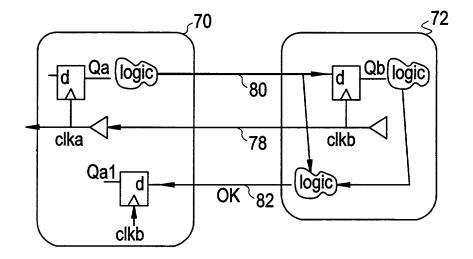


FIG. 7



clock



FIG. 8

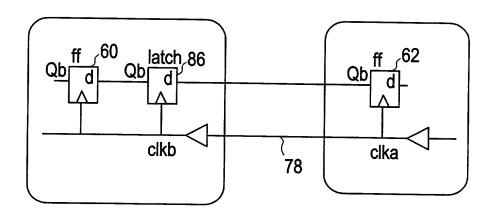


FIG. 9

clka
clkb
data_a

90

uncertainty range

clock

DE TRACEMO!

SEP 2 6 2002



FIG. 10

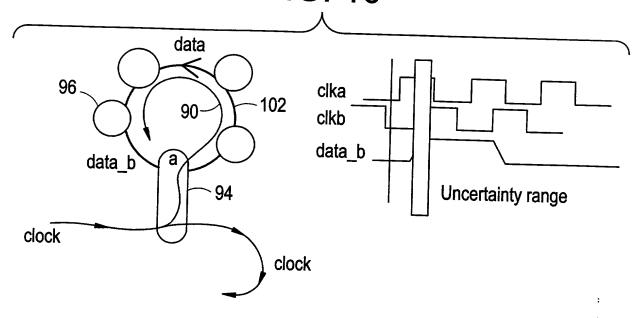


FIG. 11 local_clock ____110 -114 data_in local_data_out 116 data from previous member - data clk · - clock 112

FIG. 12 116 118 120 122

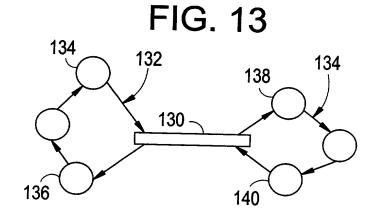




FIG. 14

3 near 154 FIG. 15 6 far

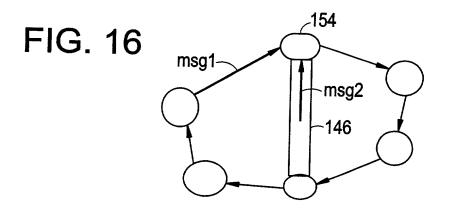




FIG. 17

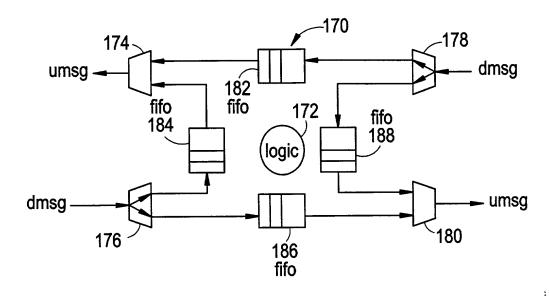
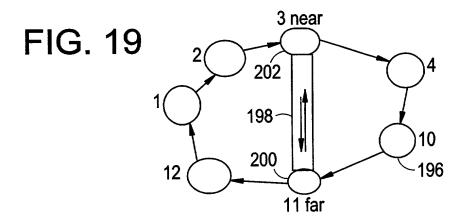


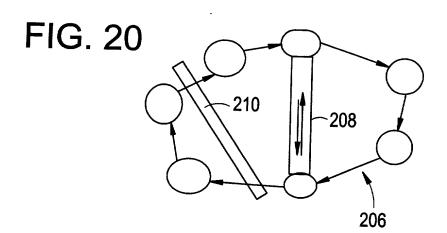
FIG. 18

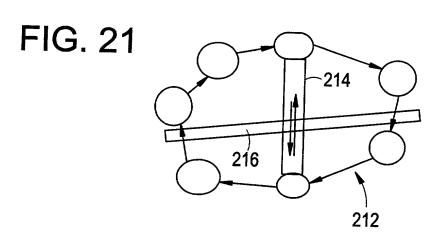
194

near far









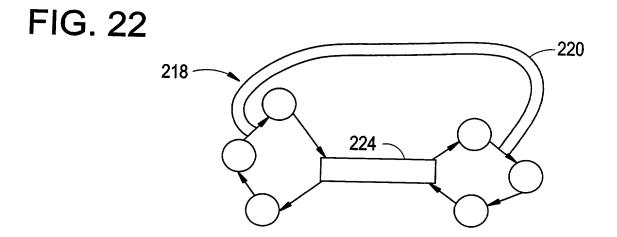




FIG. 23

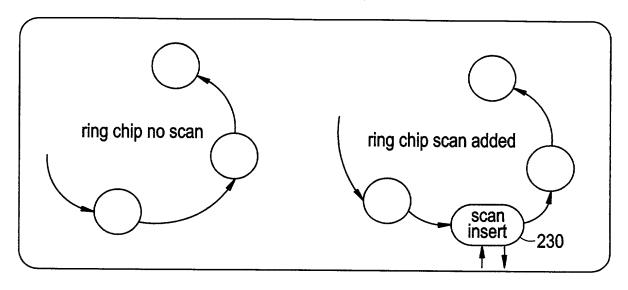


FIG. 24

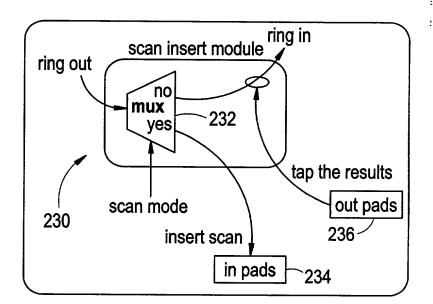


FIG. 25

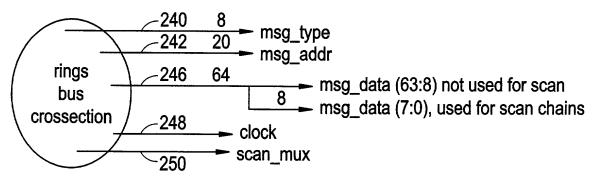




FIG. 26

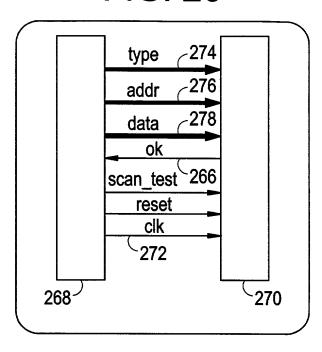


FIG. 27

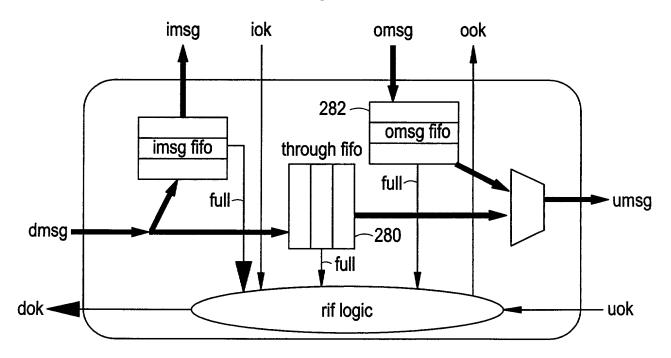




FIG. 29

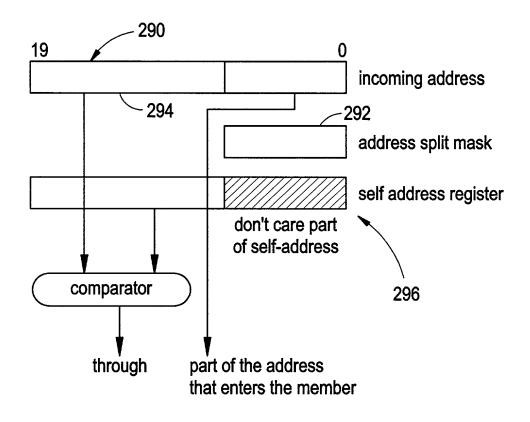




FIG. 30

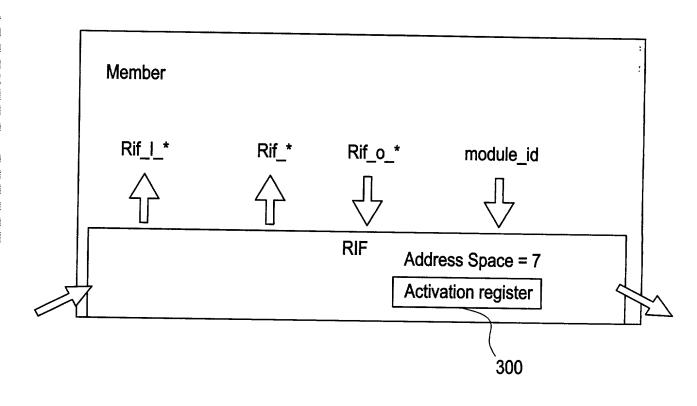




FIG. 31

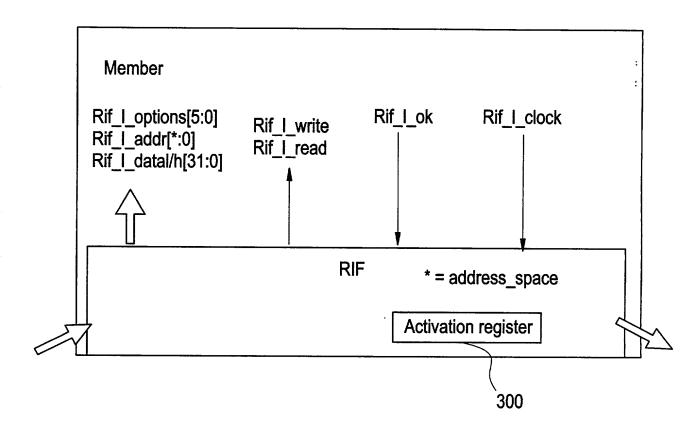




FIG. 32

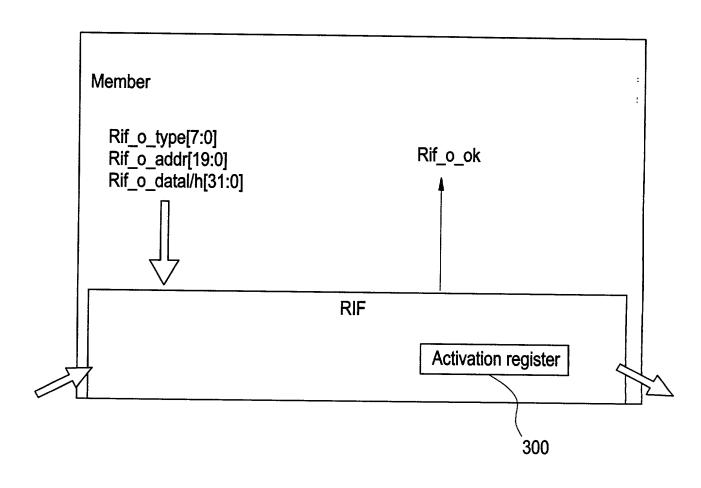
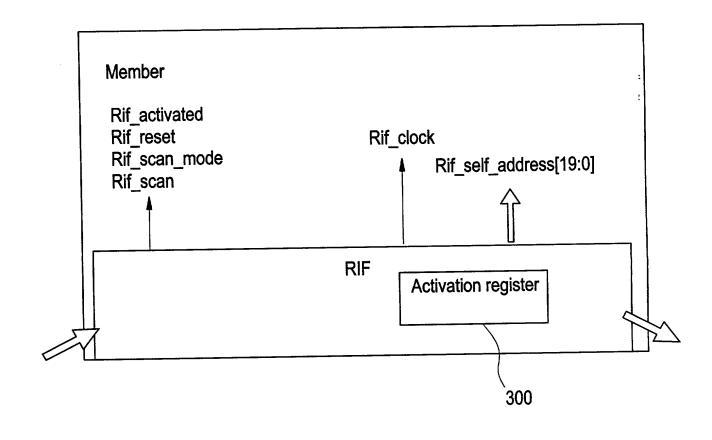




FIG. 33





17/64

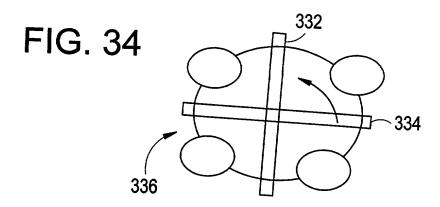
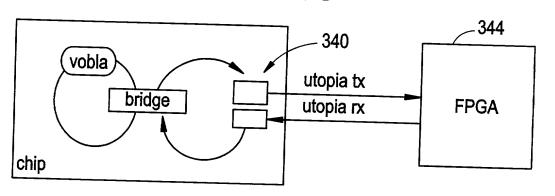
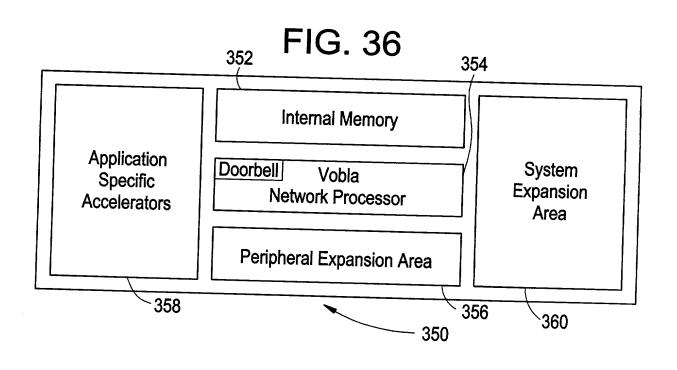
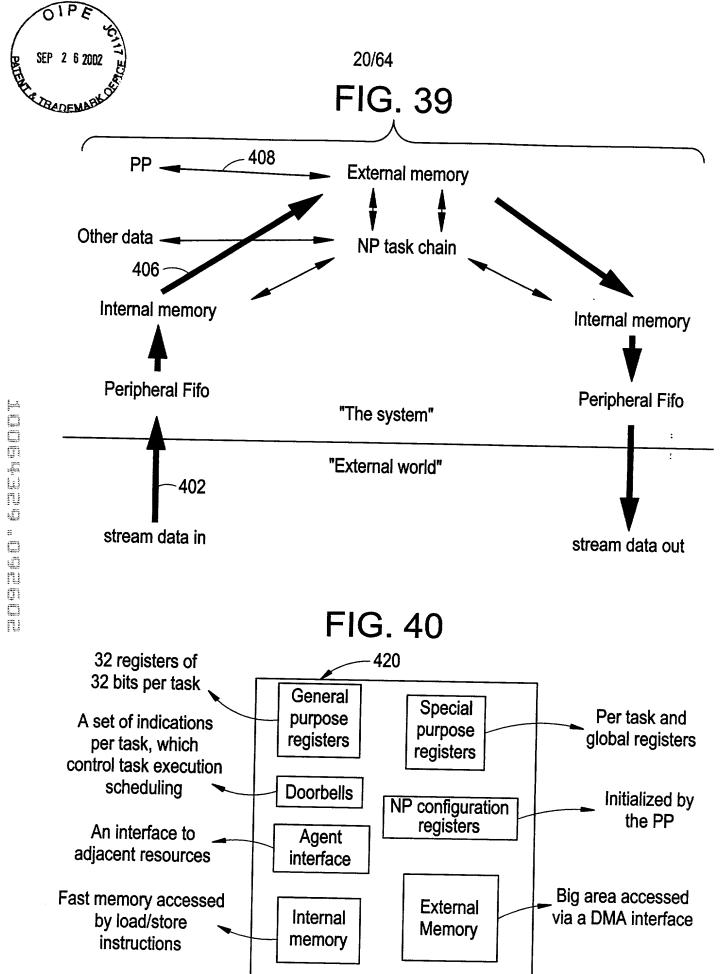


FIG. 35





ĺ

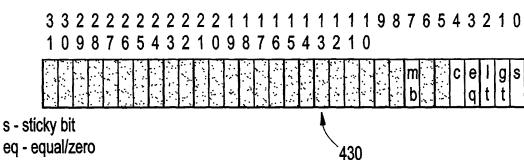




21/64

FIG. 41

R1 register



eq - equal/zero

It - less then/negative

gt - greater then/positive

c - carry

MINDEX SPR

(spr index - 3)

mb - reflection of the RAM mult-reader busy indication

FIG. 42

1098765432109876543210

REFETCH SPR **NEXT_REFETCH** REFETCH 440 (spr index - 0) 1098765432109876543210 DOOR TASK SPR UMASK : **CTID** NTID COUNT 442 (spr index - 1) 119876543210 10987654 3210987 654 D A B TRAP SPR A B (spr index - 2) 111119876543210 3 3 2 2 2 2 2 2 2 2 2 1 1 1 765432109876543210

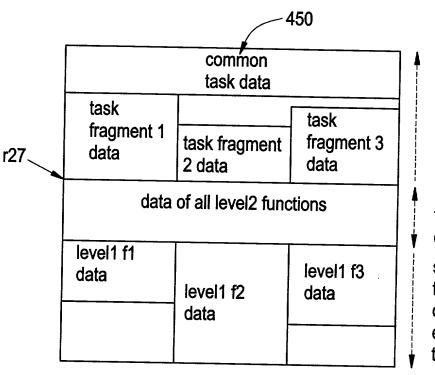
INDEX2

INDEX1

446



FIG. 43

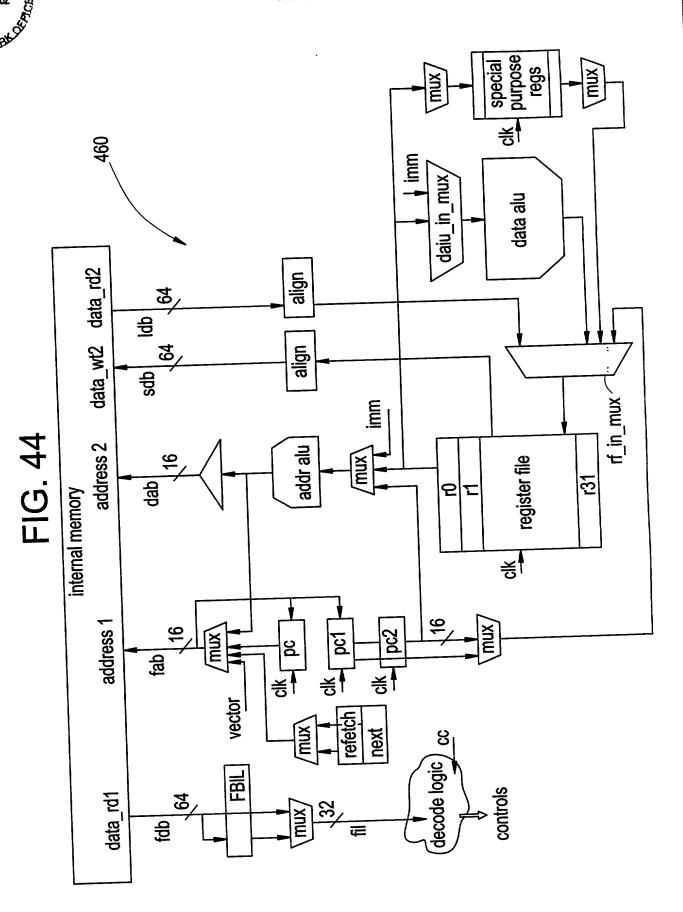


size of level0 frame part is different for each task type

size of level2 frame part is constant size of level1

frame part is different per each task type





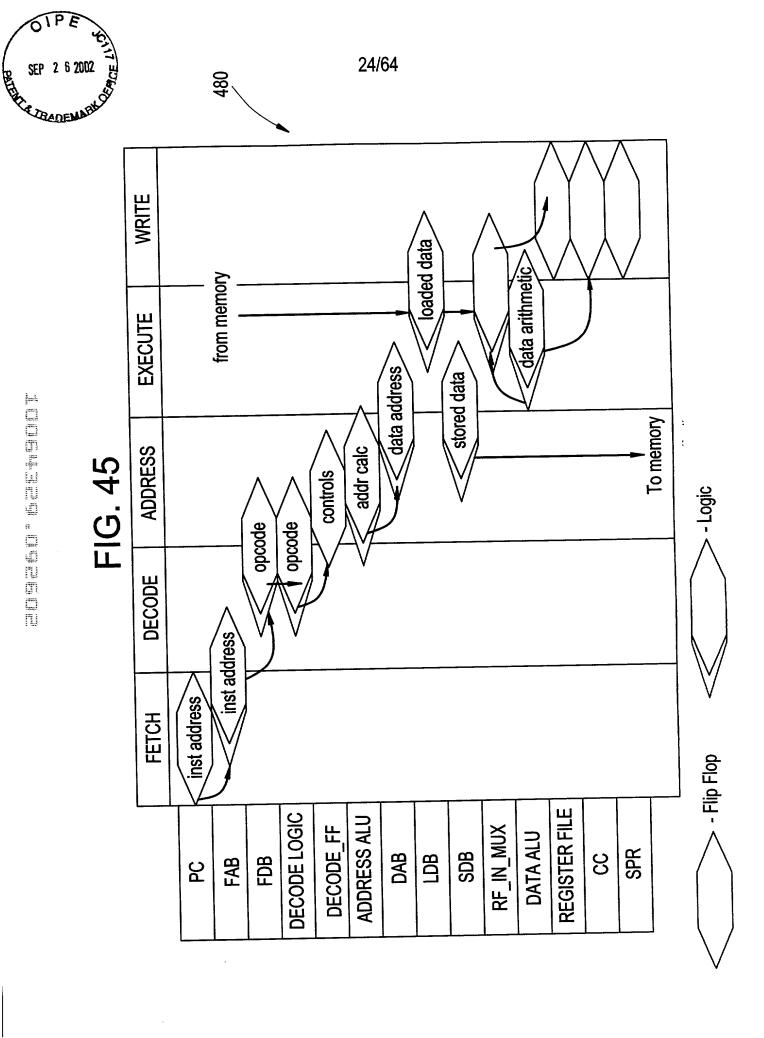




FIG. 46

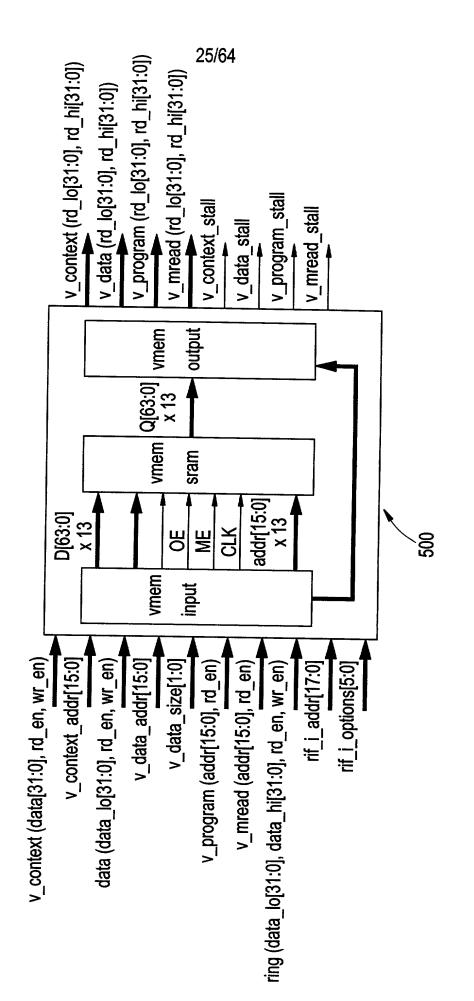
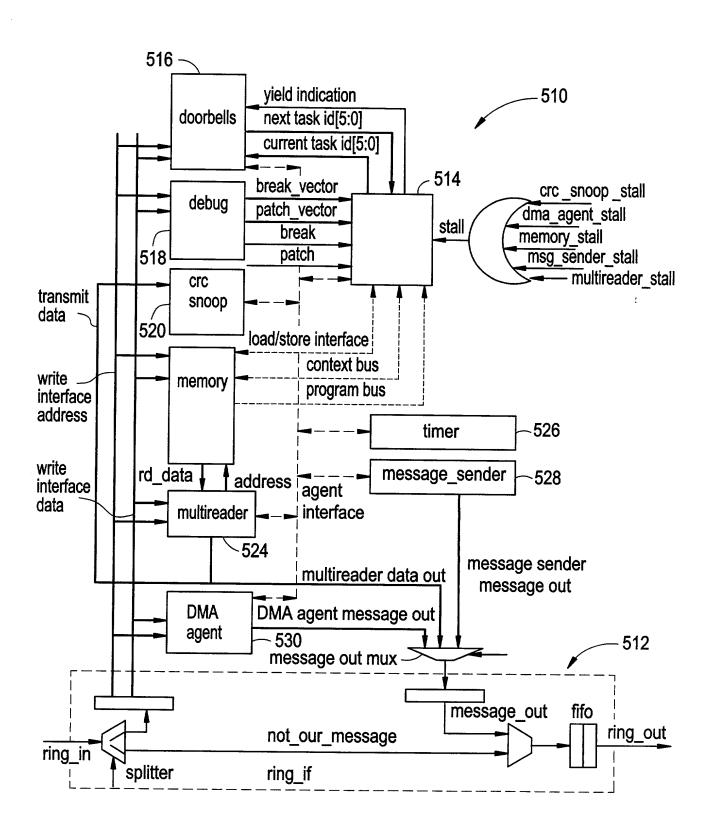
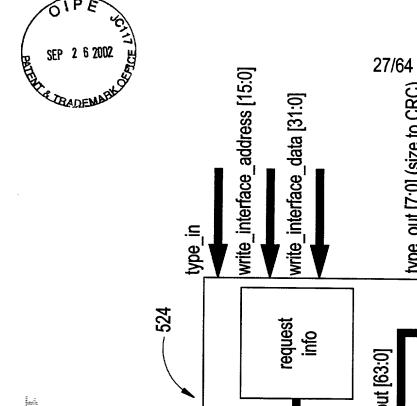






FIG. 47





data_out [63:0] (also to CRC) type_out [7:0] (size to CRC) address_out [23:0] 읒 ok2drive reset message encoder output data_out [63:0] des_add [23:0] data_out counter FIG. 48 message decoder input byte count source_add [15:0] memory interface & data packer request aligner Vobla entry vobla_multiread_busy vobla_multiread_stall mem_data_out [63:0] mr address [17:0] last_in_transfer agent interface last_in_frame calculate_crc mem_stall mr_rd crc_stall doous memory Vobla CRC

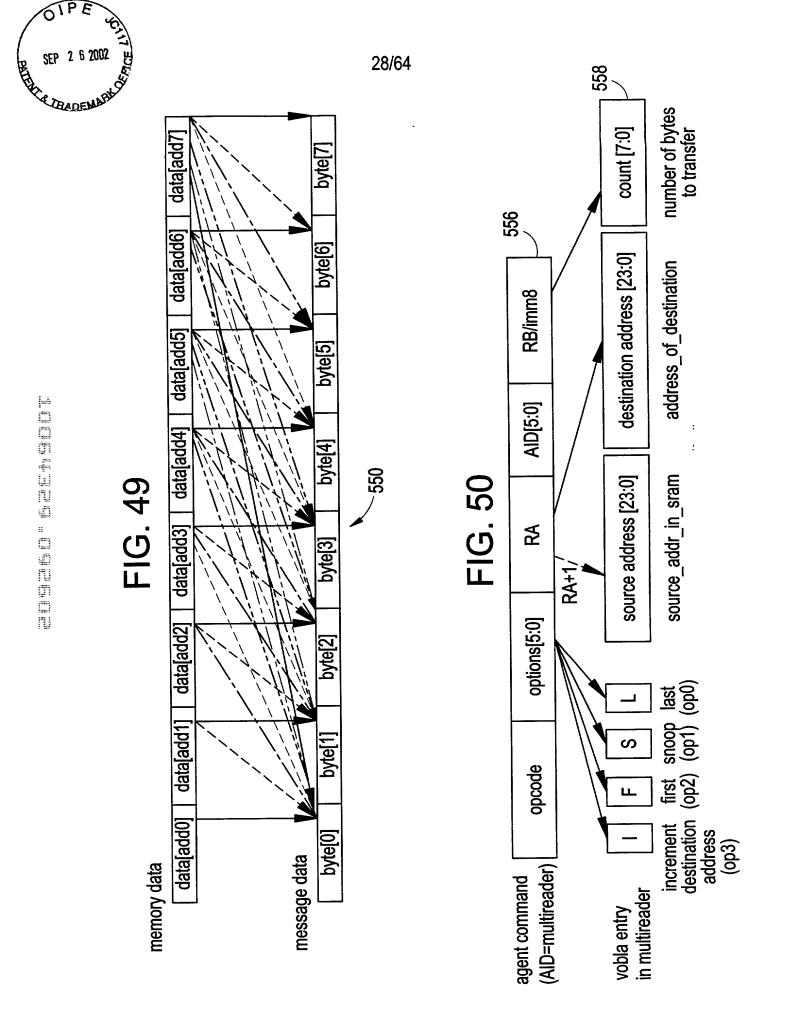
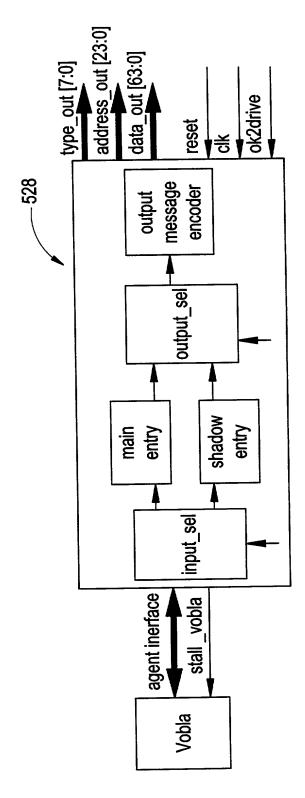




FIG. 51



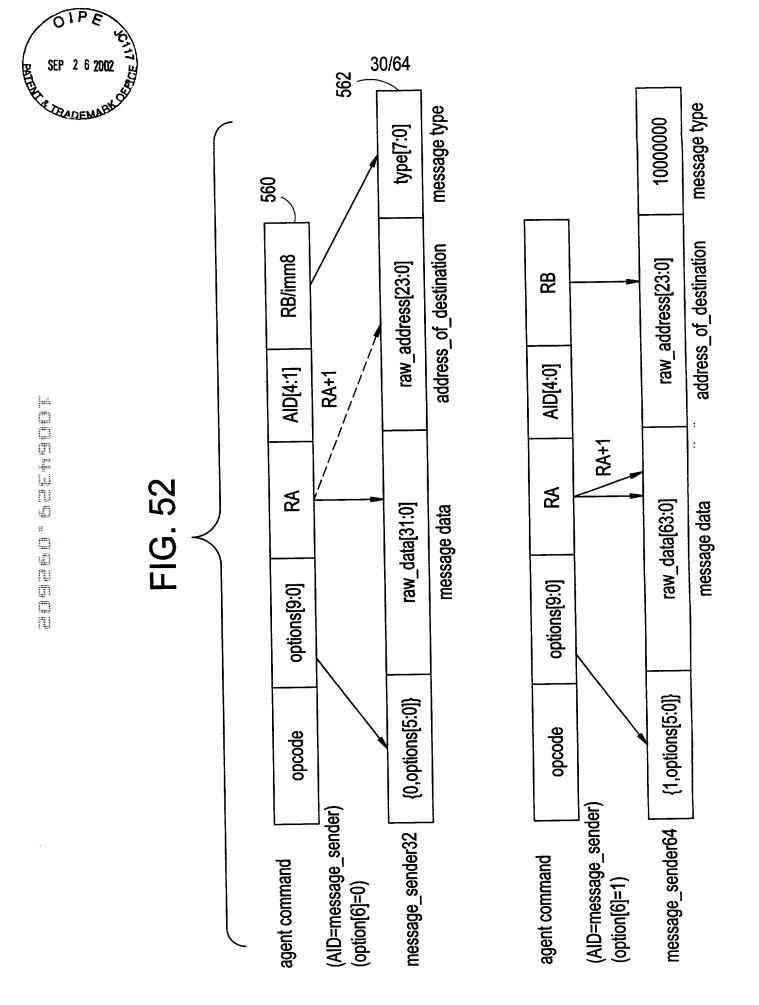




FIG. 53

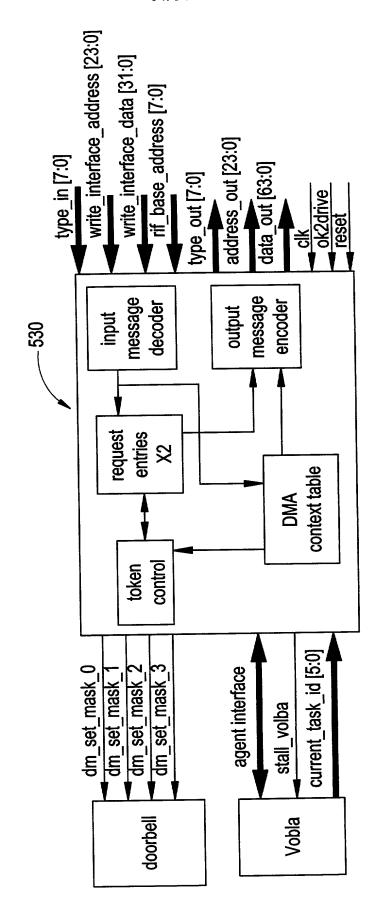




FIG. 54

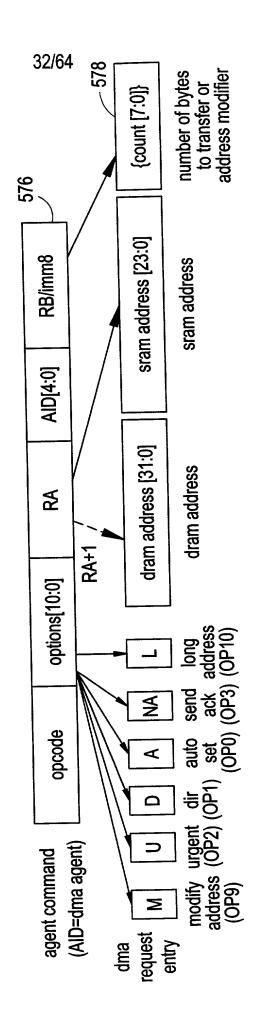




FIG. 55

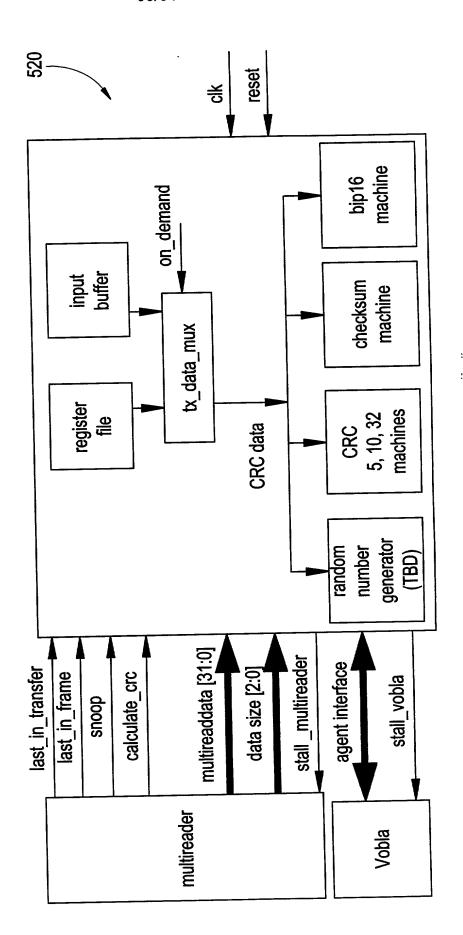
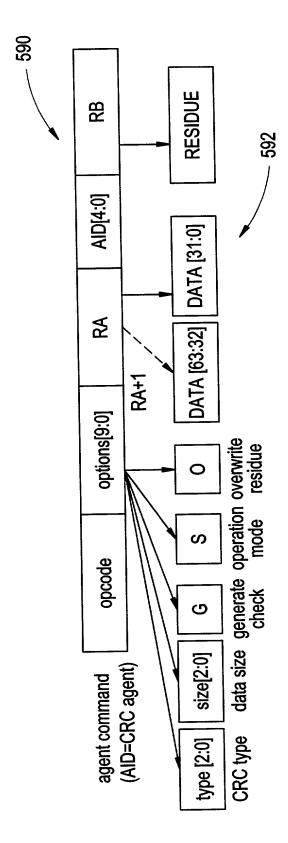




FIG. 56



:



FIG. 57

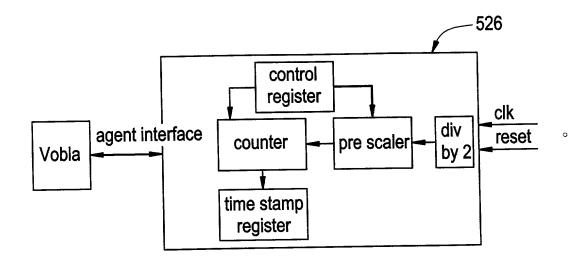
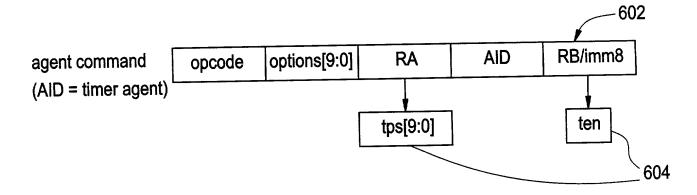
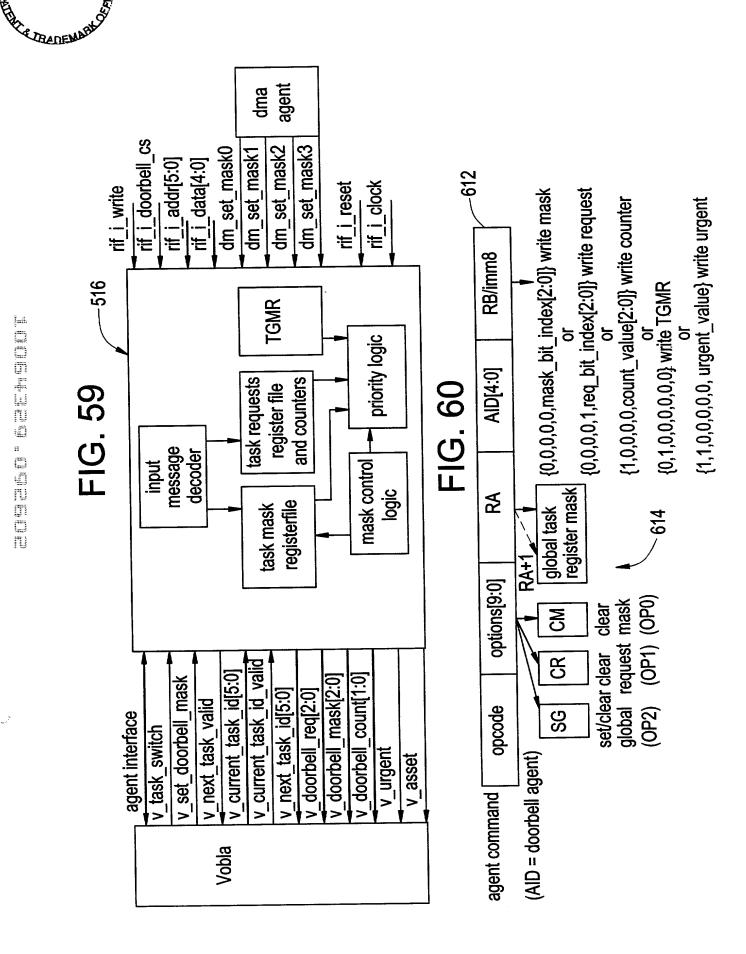
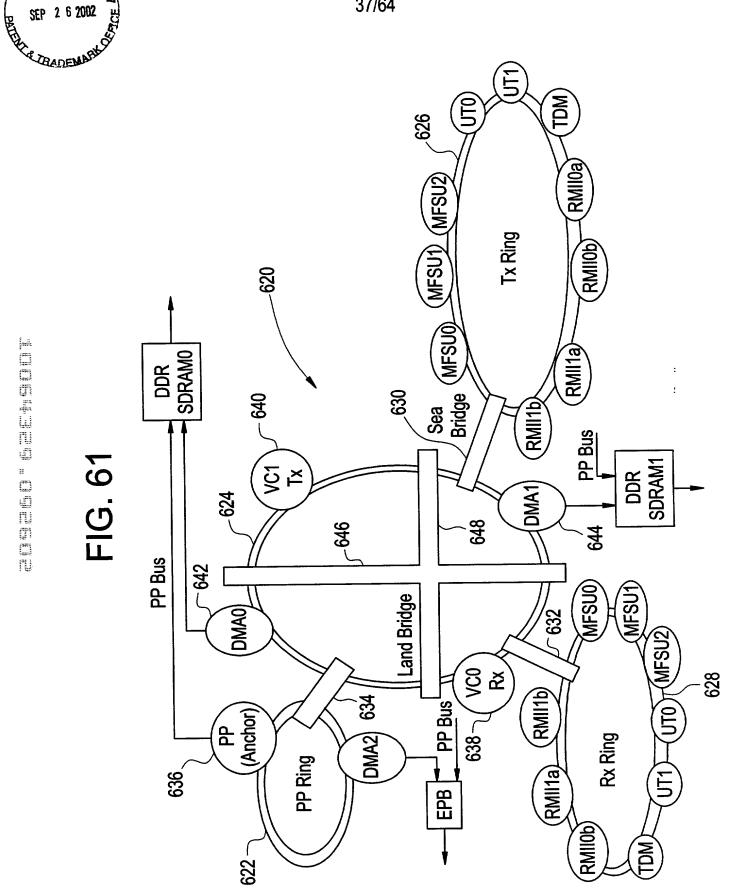


FIG. 58



2 6 2002





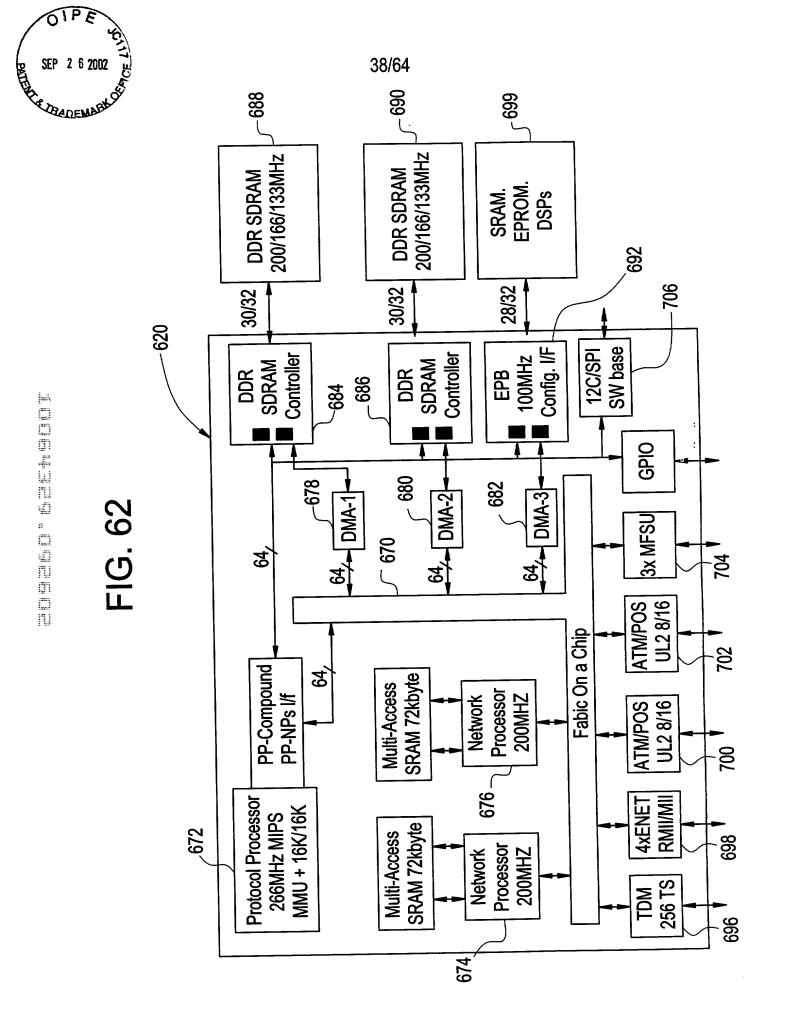




FIG. 63

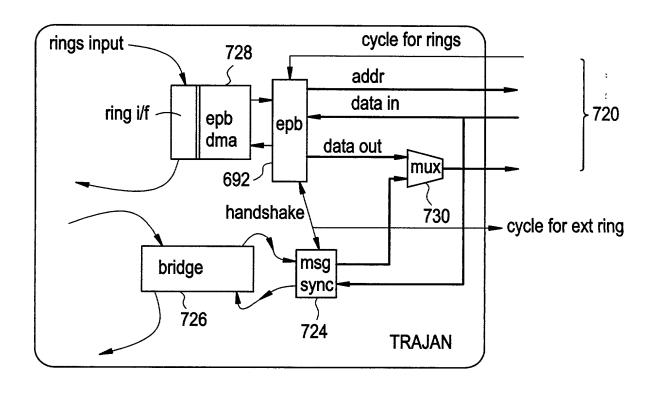
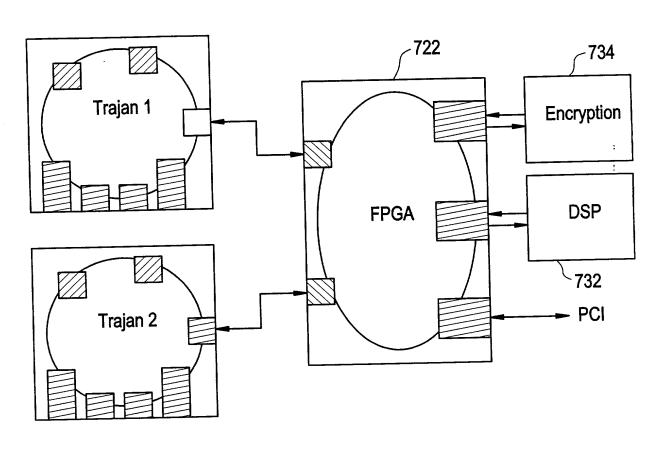




FIG. 64



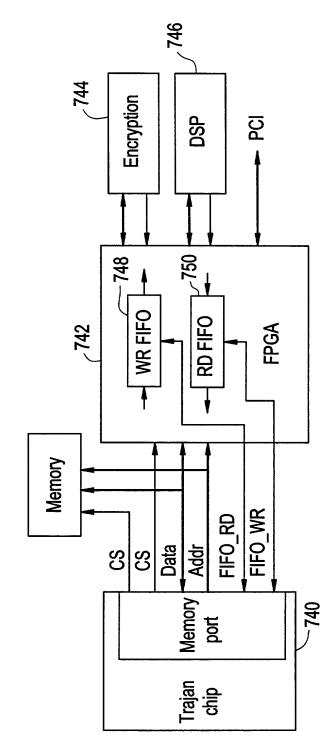
Processor

Functional unit

External ring interface



FIG. 65



:



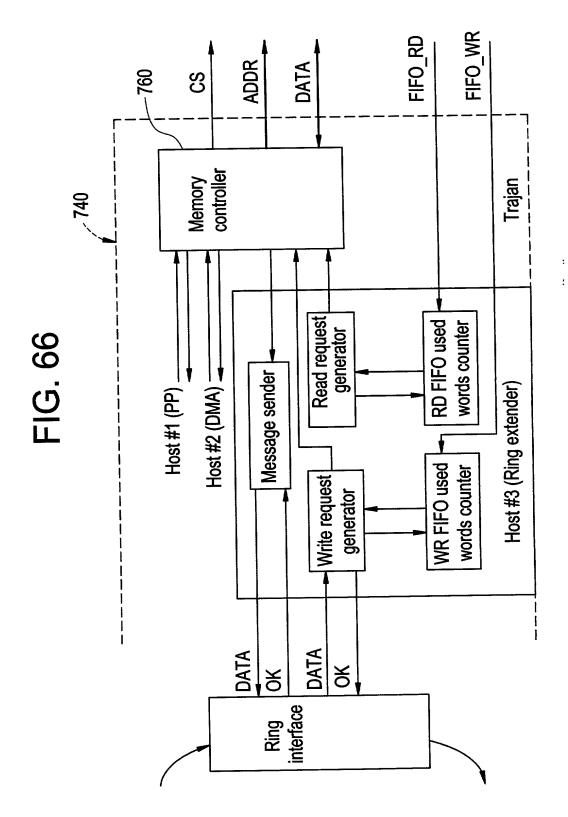
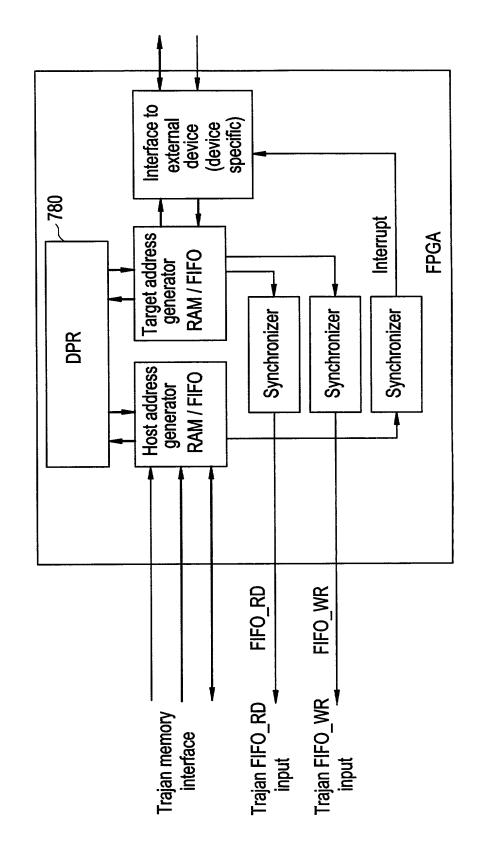




FIG. 67



:



FIG. 68

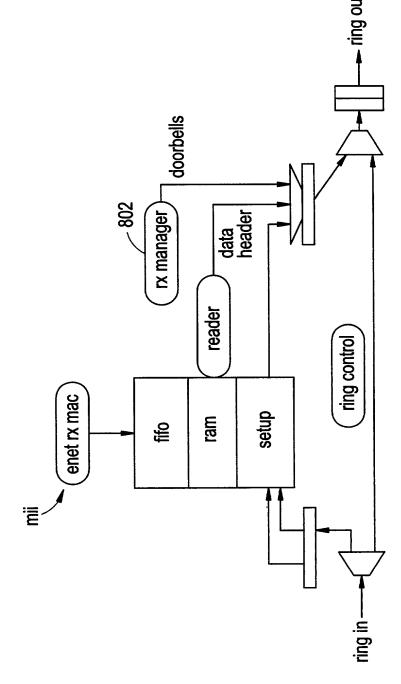




FIG. 69

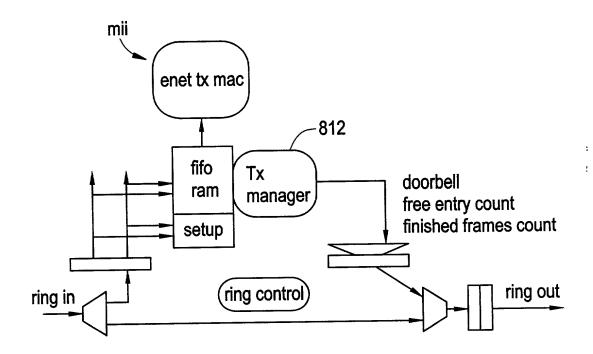
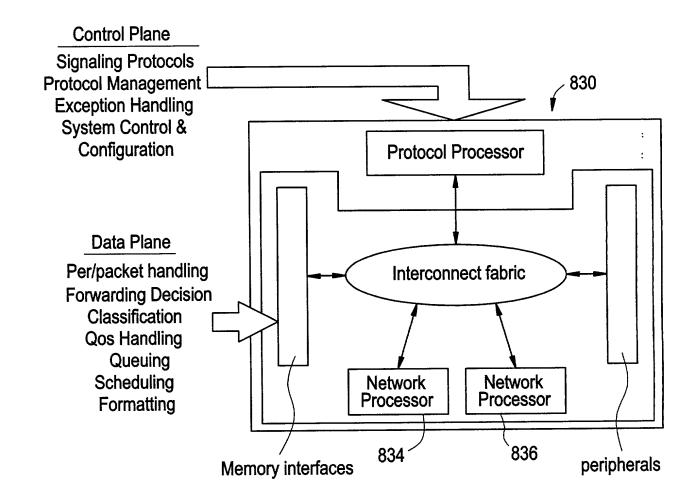
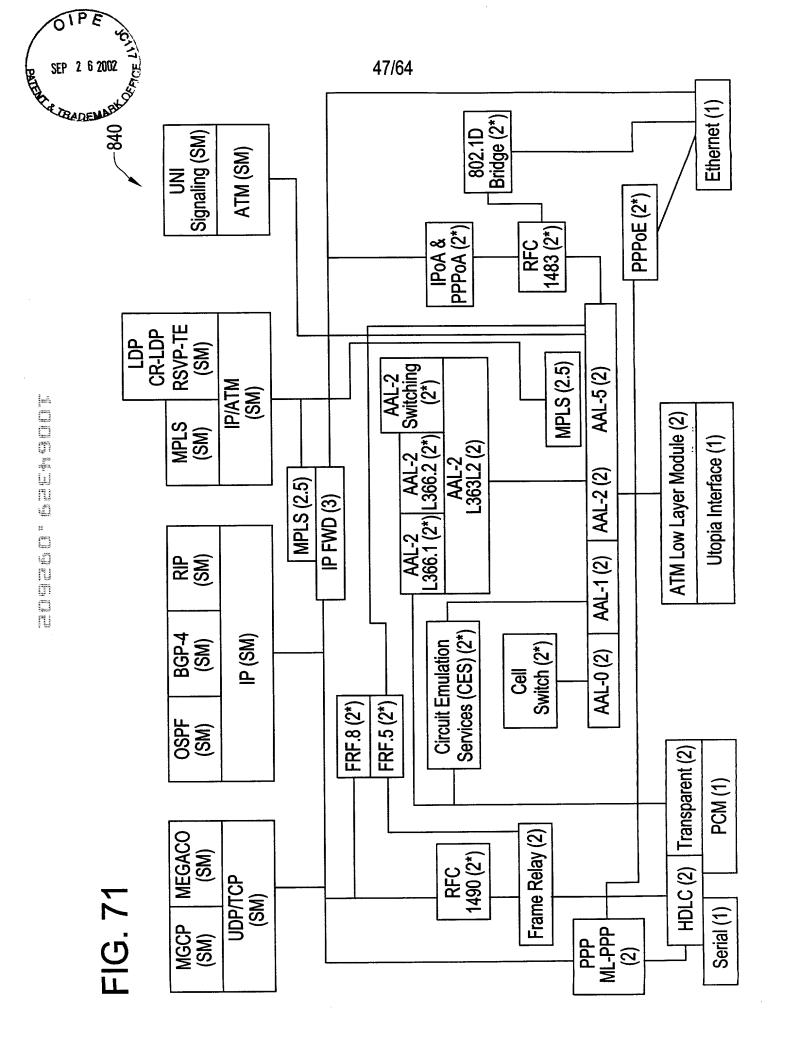




FIG. 70





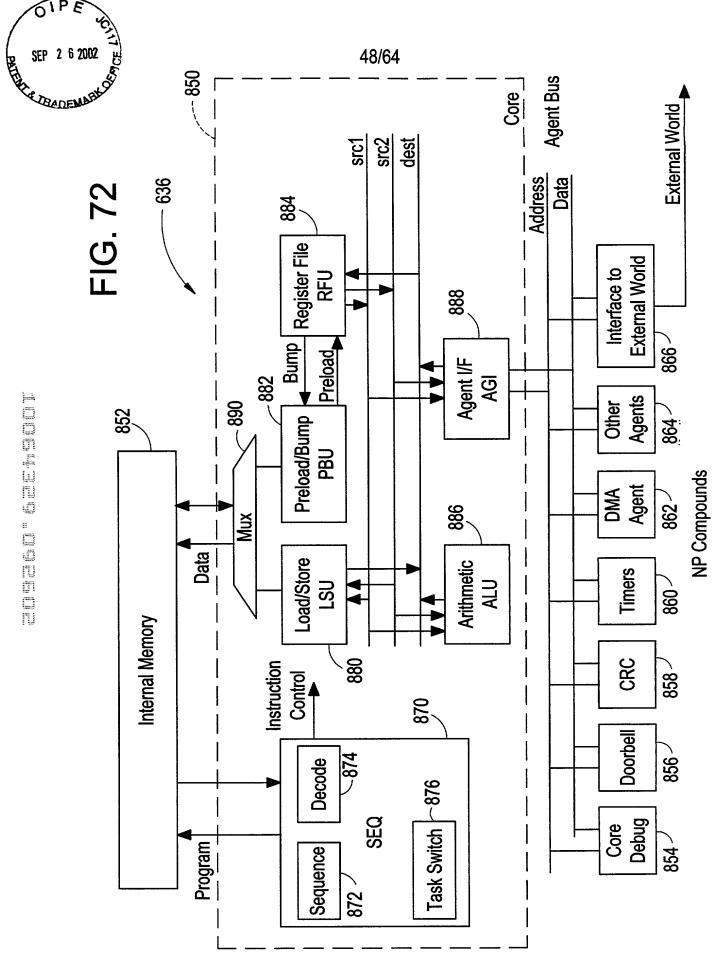




FIG. 74

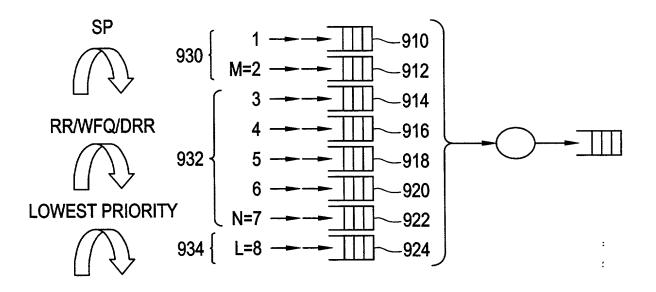
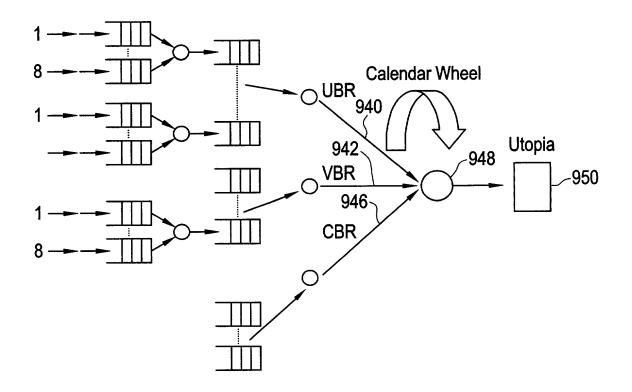
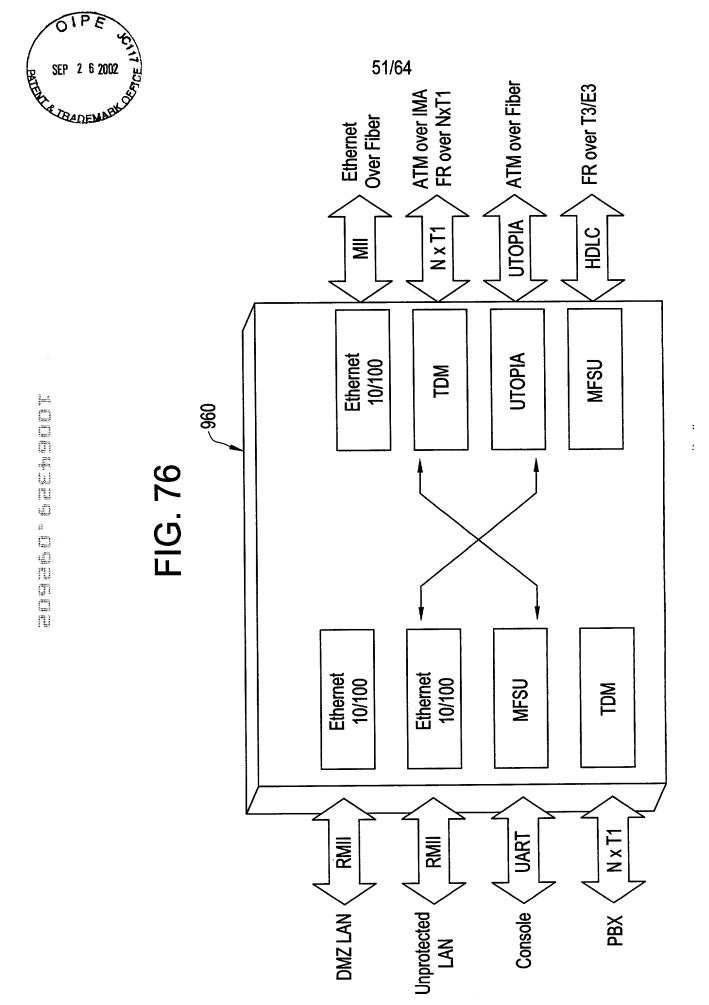
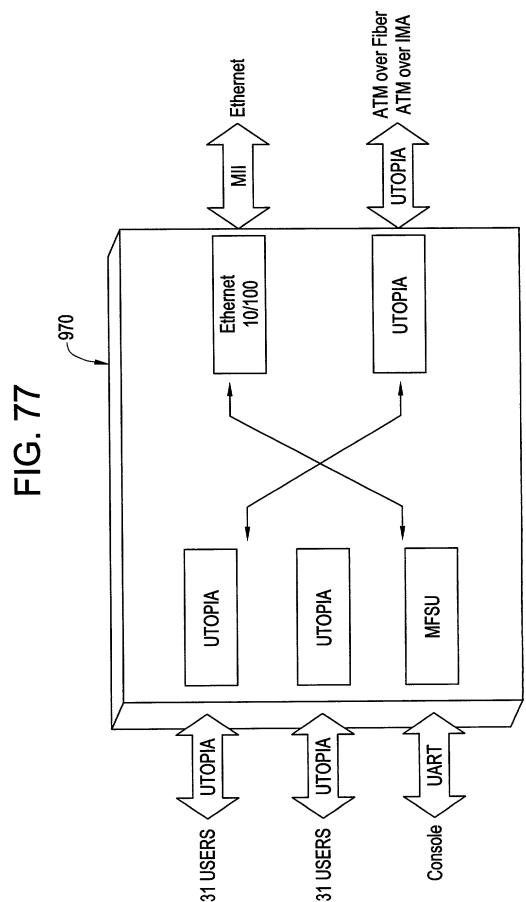


FIG. 75

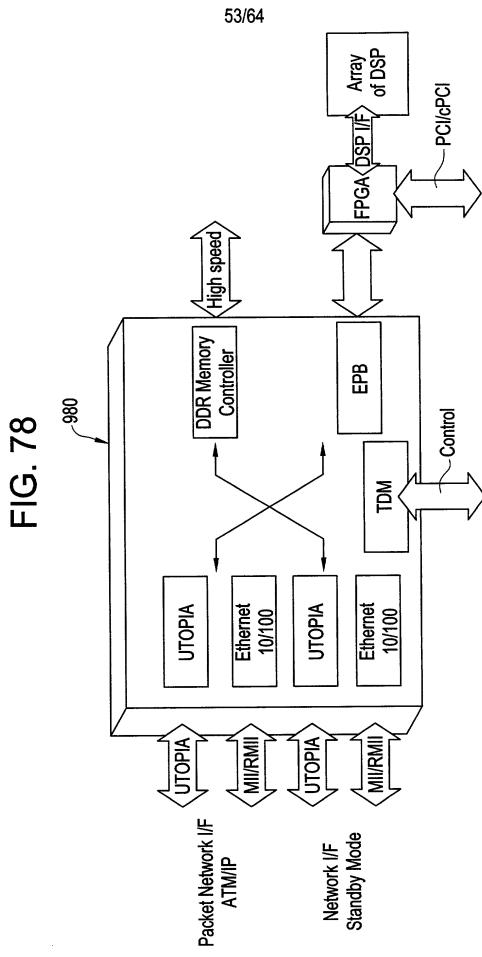




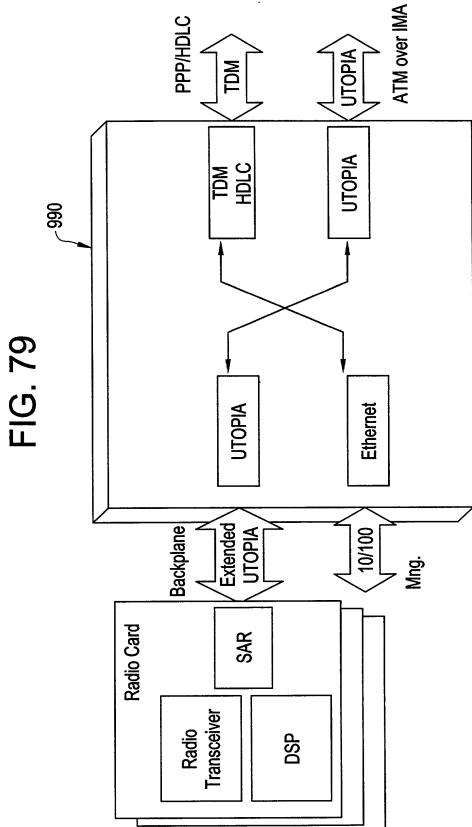


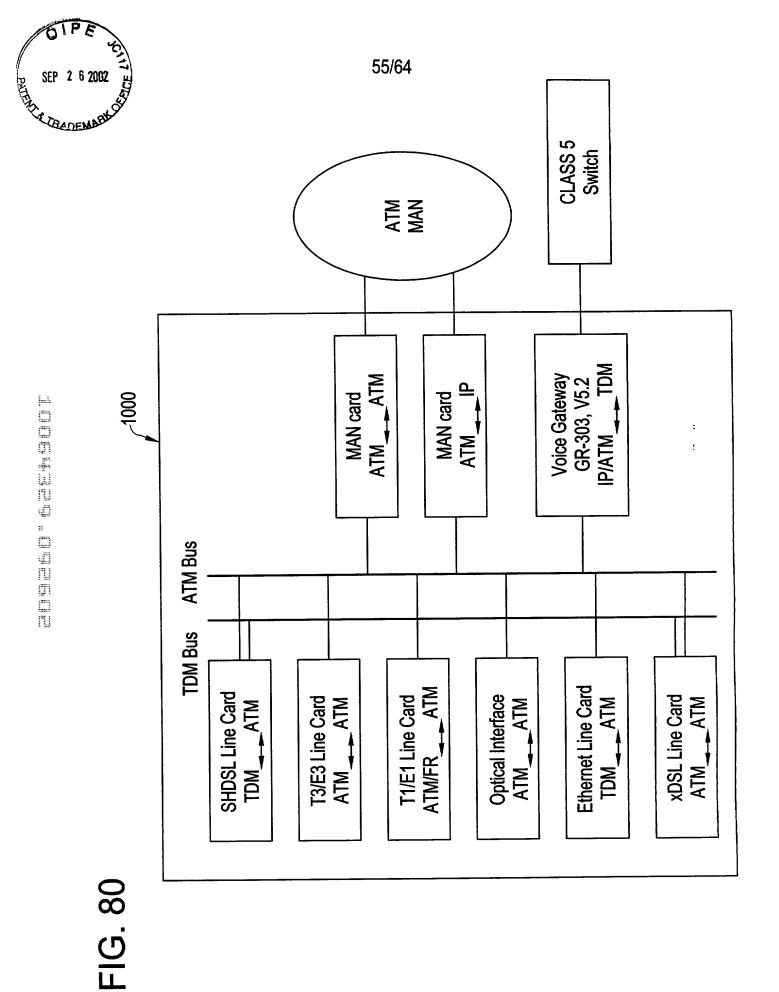


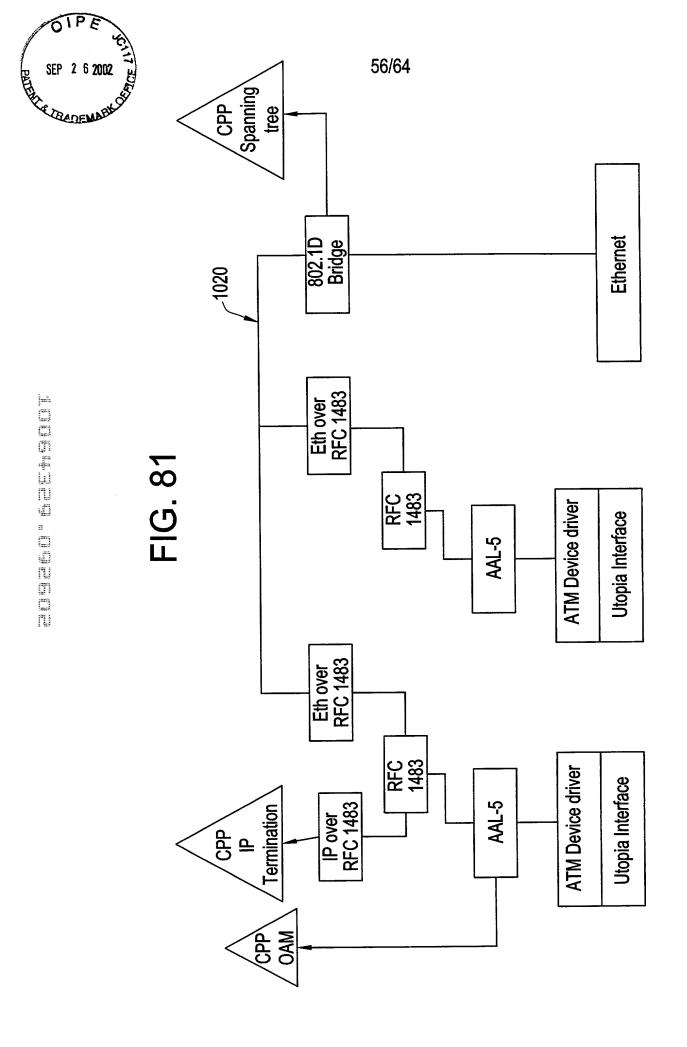
52/64

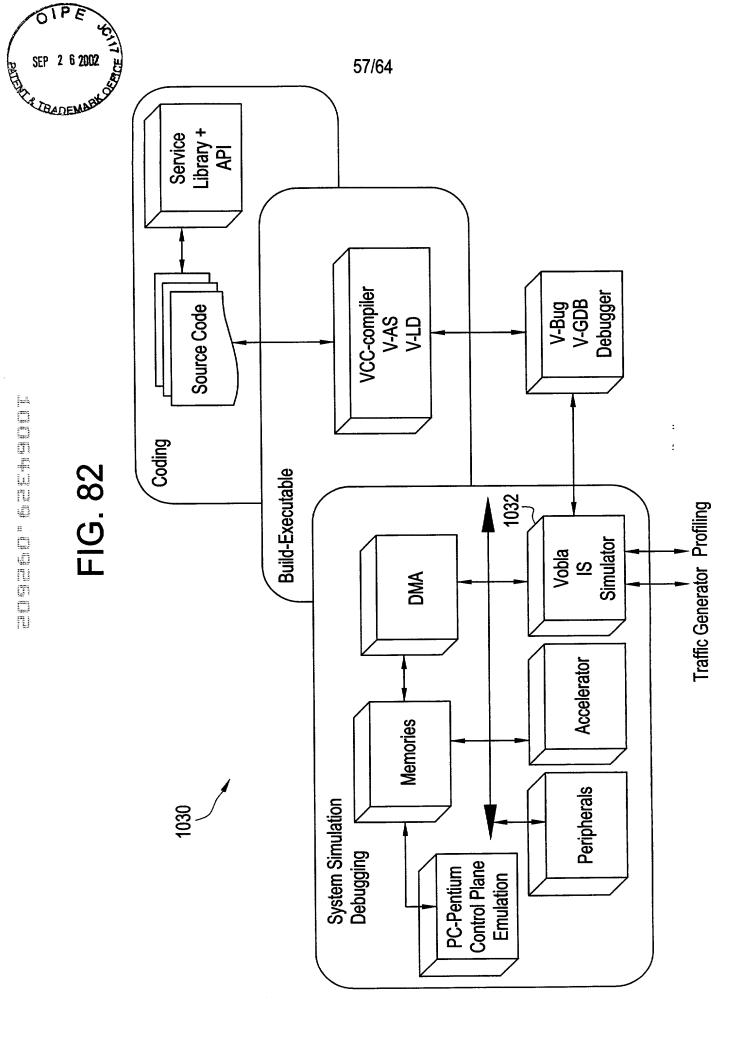


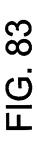












2 6 2002

THE TRANSMAN

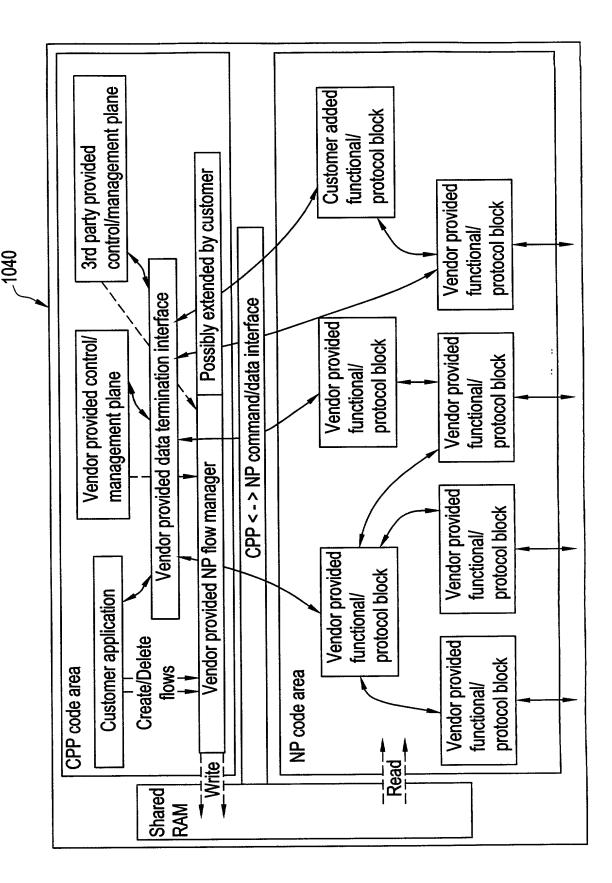
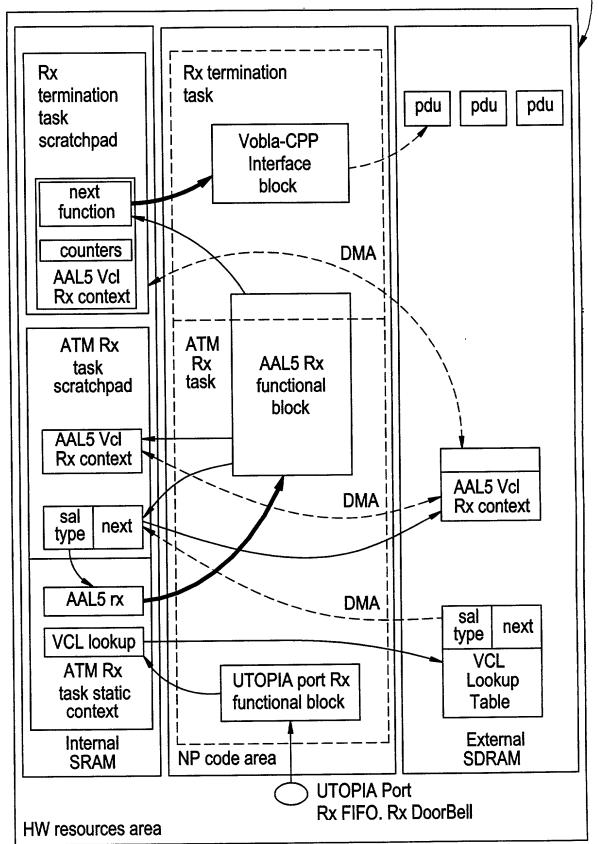
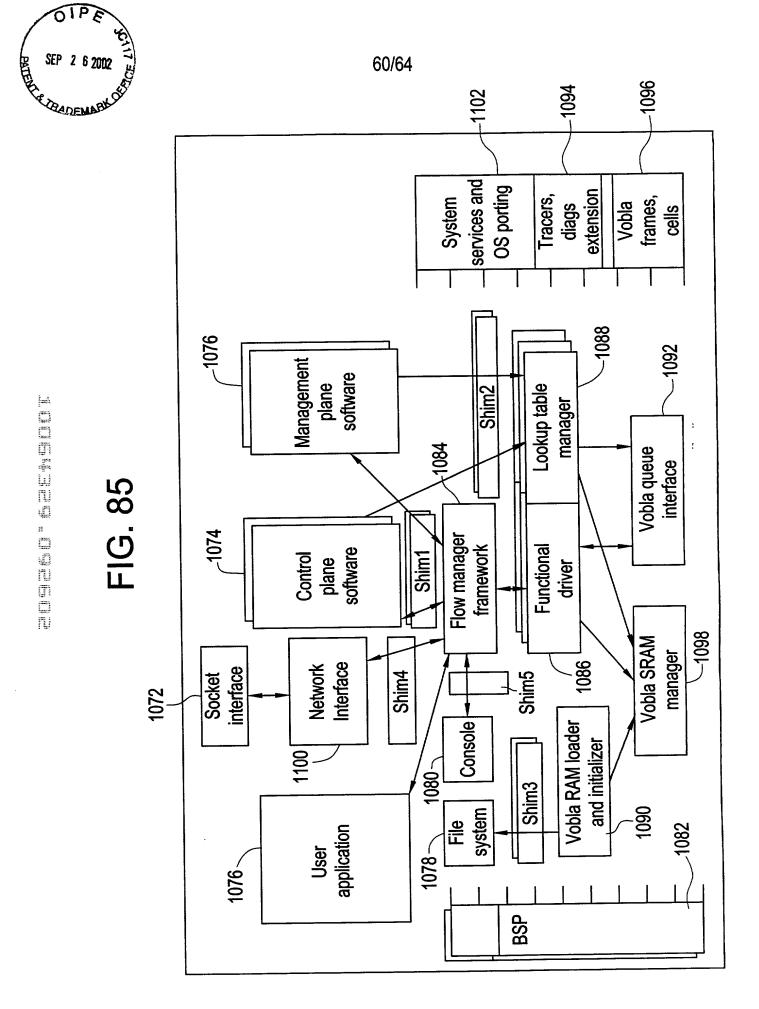


FIG. 84

1050





SEP 2 6 2002

TADEMARKS

FIG. 86

1200

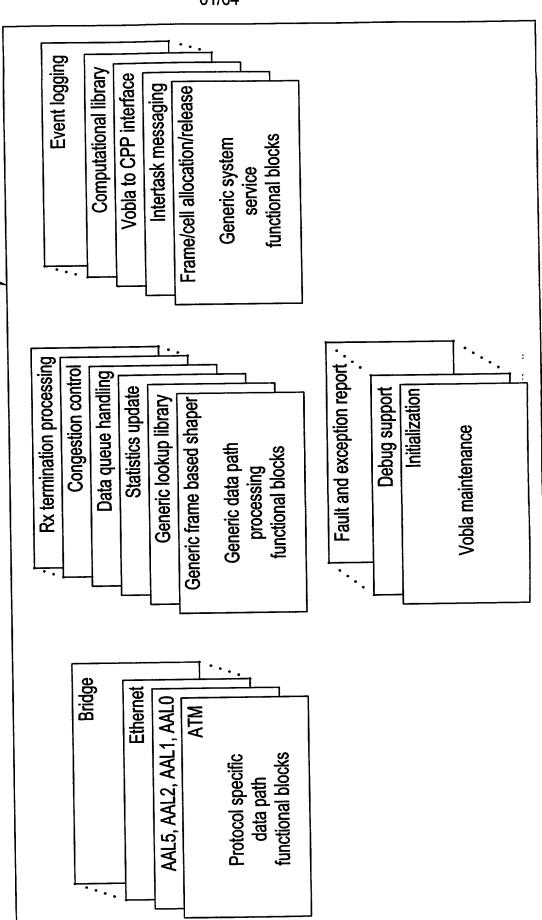




FIG. 87

PRIOR ART

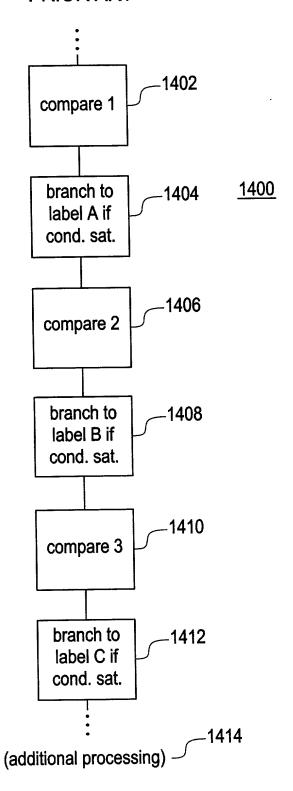




FIG. 88

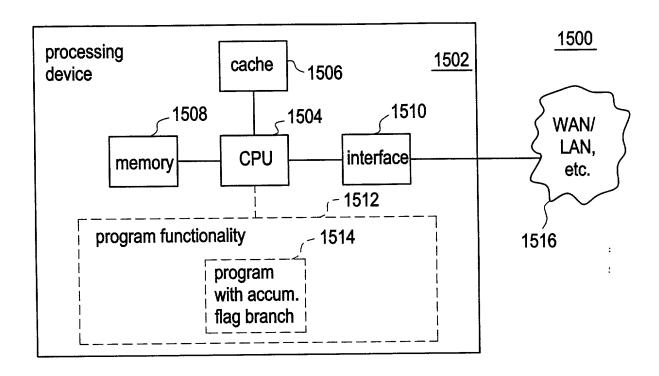


FIG. 89

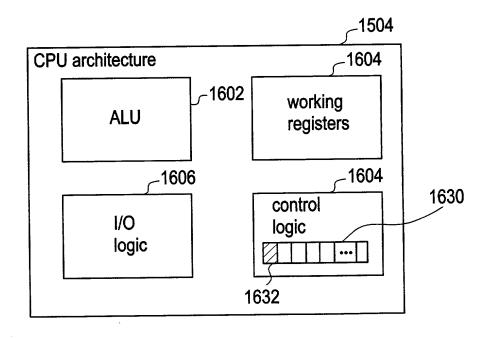




FIG. 90

